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ECE 5484, Homework 3

1. How many bits are required to address a 4M × 16 main memory if

a. Main memory is byte-addressable?

4 x 220 x 2 = 22 x 2 20 x 21 = 223 bytes

Therefore, 23 bits are needed for an address.

b. Main memory is word-addressable? (For part b, assume a 16-bit word.)

4 x 220 = 22 x 220 = 222 words

Therefore, 22 bits are needed for an address.

2. You want to use 256 x 8 RAM chips to provide a memory capacity of 4096 bytes.

a. How many chips will you need?

Number of bytes: 256 \* 1 = 256 bytes

Number of chips= 4096 / 256 = 16 chips

b. How many bits will each address contain?

Since 4096 = 212

Therefore, each address contains 12 bits

c. How many address lines must go to each chip?

Since number of bytes = 256 = 28

Number of address lines = 8 address lines

d. How many address lines must be decoded for the chip select inputs? In other words, specify the size of the decoder.

Since we have 16 chips = 24, so we need 4 address lines to select the chip.

3. A digital computer has a memory unit with 40 bits per word. The instruction set consists of 165 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.

a. How many bits are needed for the opcode?

We need room for each one instruction, meaning 165 unique opcodes

165 = 2n, log165 = log2n, log165 = nlog2, therefore n = log165/log2 = 7.36 ≈ 8

Since 28 = 256 and 27 = 128, therefore we will take the 8 bits to have enough space for 165

Therefore, we need 8 bits for the opcode.

b. How many bits are left for the address part of the instruction?

Number of bits left for address part = 40 – 8 = 32 bits

c. What is the maximum allowable size for memory?

232 words

d. What is the largest unsigned binary number that can be accommodated in one word of memory?

240 – 1 words

4. (a) Load 105

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Step** | **RTN** | **PC** | **IR** | **MAR** | **MBR** | **AC** |
| (initial values) |  | 100 | ― | ― | ― | ― |
| Fetch | MAR ← PC | 100 | ― | 100 | ― | ― |
|  | IR ← M[MAR] | 100 | 1105 | 100 | ― | ― |
|  | PC ← PC + 1 | 101 | 1105 | 100 | ― | ― |
| Decode | MAR ← IR[11-0] | 101 | 1105 | 105 | ― | ― |
|  | (Decode IR[15-12]) | 101 | 1105 | 105 | ― | ― |
| Get operand | MBR ← M[MAR] | 101 | 1105 | 105 | 00F3 | ― |
| Execute | AC ← MBR | 101 | 1105 | 105 | 00F3 | 00F3 |

(b) Subt 104

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Step** | **RTN** | **PC** | **IR** | **MAR** | **MBR** | **AC** |
| (initial values) |  | 101 | 1105 | 105 | 00F3 | 00F3 |
| Fetch | MAR ← PC | 101 | 1105 | 101 | 00F3 | 00F3 |
|  | IR ← M[MAR] | 101 | 4104 | 101 | 00F3 | 00F3 |
|  | PC ← PC + 1 | 102 | 4104 | 101 | 00F3 | 00F3 |
| Decode | MAR ← IR[11-0] | 102 | 4104 | 104 | 00F3 | 00F3 |
|  | (Decode IR[15-12]) | 102 | 4104 | 104 | 00F3 | 00F3 |
| Get operand | MBR ← M[MAR] | 102 | 4104 | 104 | 00A3 | 00F3 |
| Execute | AC ← AC - MBR | 102 | 4104 | 104 | 00A3 | 0050 |

(c) Store 104

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Step** | **RTN** | **PC** | **IR** | **MAR** | **MBR** | **AC** |
| (initial values) |  | 102 | 4104 | 104 | 00A3 | 0050 |
| Fetch | MAR ← PC | 102 | 4104 | 102 | 00A3 | 0050 |
|  | IR ← M[MAR] | 102 | 2104 | 102 | 00A3 | 0050 |
|  | PC ← PC + 1 | 103 | 2104 | 102 | 00A3 | 0050 |
| Decode | MAR ← IR[11-0] | 103 | 2104 | 104 | 00A3 | 0050 |
|  | (Decode IR[15-12]) | 103 | 2104 | 104 | 00A3 | 0050 |
| Get operand | (not necessary) | 103 | 2104 | 104 | 00A3 | 0050 |
| Execute | MBR ← AC | 103 | 2104 | 104 | 0050 | 0050 |
|  | M[MAR] ← MBR | 103 | 2104 | 104 | 0050 | 0050 |

5. Scavenger Hunt: Two pioneers of early computers and computer organization were Howard H. Aiken and John von Neumann. Answer the questions below regarding Aiken and von Neumann. *Cite sources used for your answers*.

a. Is Aiken or is von Neumann associated with the so-called Princeton architecture?

von Neumann

b. Is Aiken or is von Neumann associated with the so-called Harvard architecture?

Aiken

c. In your own words, what is the key feature of a Princeton architecture computer compared to the Harvard architecture?

Princeton architecture has only one bus which is used for both data transfers and instruction fetches, and therefore data transfers and instruction fetches must be scheduled (they cannot be performed at the same time). However, Harvard architecture has separate data and instruction busses, allowing transfers to be performed simultaneously on both busses.

d. Does the MARIE architecture owe more to Aiken or von Neumann? In your own words, briefly justify your answer

MARIE architecture owes more to von Neumann since it uses the van Neumann architecture with a simple instruction set.

References

1. John Louis Von Neumann. (n.d.). Retrieved from <https://history.computer.org/pioneers/von-neumann.html>
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3. Stanley, T. D., Wong, L. K., Prigmore, D., Benson, J., Fishler, N., Fife, L., & Colton, D. (2007). From Archi Torture to architecture: Undergraduate students design and implement computers using the Multimedia Logic emulator. *Computer Science Education,* *17*(2), 141-152. doi:10.1080/08993400601165735